SynthWorks℠
Expert VHDL Training for Hardware Design and Verification

Quick VHDL Introduction

2 Days: 60% Lecture, 40% Lab **Basic Level**

Overview

Comprehensive VHDL Introduction shortened for support engineers and managers who only need to understand the basics of using VHDL in a design environment. Only recommended for design and verification engineers when they plan on immediately following it with additional training.

Through two days of lecture, exercises, and labs, students will learn basic VHDL coding and simulation techniques. Lectures contain examples that show both syntax and coding style guidelines. Exercises provide immediate reinforcement of lecture materials. Labs give students hands-on experience writing VHDL code and running your simulator.

Course Objectives

Upon completion of this course, students will be able to:

- Understand VHDL keywords, syntax and coding styles necessary for logic design
- Write simple VHDL models, netlists, and testbenches
- Read and understand more complex VHDL models

Course Outline

Day 1

A Quick Introduction
Lab 1: Simple RTL and Testbench
Data Types
Operators
Concurrent Statements
Sequential Statements
Lab 2: Clock and Reset
Lab 3: RTL and Testbench

Day 2

RTL Essentials
Statemachine Coding Techniques
Lab 4: RTL Code
Data Objects
Designing with VHDL
Lab 5: Coding an FSM
Lab 6: Creating Hierarchy

VHDL Introduction

Prerequisites

None. Offered as a first course in VHDL. It is recommended that students are familiar with digital design.

Follow-On Courses

Students wishing to go beyond what they learned in this course should take either or both of the following courses:

VHDL Coding Styles for Synthesis - 4 days

VHDL Testbenches and Verification - 4 days

Customization

All of our courses can be customized to meet your specific needs. Either see our website or contact us for details.

Training Approach

This hands-on, how-to course is taught by experienced hardware designers using a computer driven projector. We prefer and encourage student and instructor interaction. Questions are welcome. Bring problematic code.

Contact

To schedule a class or for more information, contact:

Jim Lewis
Director of Training
(800) 505-8435 / (800) 505-VHDL
(503) 590-4787
jim@SynthWorks.com
http://www.SynthWorks.com

Learn VHDL from a designer's perspective with SynthWorks.

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