SynthWorks
VHDL Training Experts

SynthWorks announces Methodology and Open-Source Packages for creating Constrained Random Tests in VHDL.

PORTLAND, OREGON -- (Business Wire) – February 7, 2011 – SynthWorks, a leader in VHDL training, announces its proven VHDL based constrained random and coverage driven random testbench methodology. At the heart of this methodology are packages for randomization and functional coverage that SynthWorks' has released as an open source download.

Constrained Random Testing

Constrained random testbenches create tests by successively randomizing sequences (transactions or groups of transactions) that are valid for a particular environment. This approach quickly generates test sequences saving test development time. It is particularly effective for designs where the diversity of transactions and sequences make it otherwise difficult to generate. Functional coverage counts what transactions occur, and hence, indicates when a test is done.

SynthWorks' Methodology

SynthWorks' constrained random methodology has been in use since 2006. This methodology allows you to add constrained random testing to your existing VHDL testbenches. There is no new language to learn and no throwing out your current testbench or testbench models.

SynthWorks' methodology marries randomization and functional coverage subprograms from the packages with VHDL programming constructs. Each test sequence is derived by randomly selecting either branches of code or values for operations. Randomization constraints are created using normal sequential coding techniques (such as nesting of case, if, loop, and assignment statements). Functional coverage counts which test cases are generated using subprograms (either custom or from the coverage package) or VHDL code. Functional coverage is stored in signals and can be used as randomization constraints to generate missing coverage items. SynthWorks has developed templates for common problems to accelerate test development.

Download Open Source Packages

The open source packages can be downloaded at: http://www.synthworks.com/downloads. The download includes compilation instructions and slides showing how to do basic operations.

Learning More

To learn the latest verification techniques using VHDL, including constrained and coverage driven randomization, functional coverage, transaction-based testing, bus functional modeling, self-checking,

and data structures (linked-lists, scoreboards, memories), see SynthWorks' VHDL Testbenches and Verification class at: http://www.synthworks.com/vhdl_testbench_verification.htm.

About SynthWorks

SynthWorks provides VHDL training that helps either new or experienced engineers be more effective on their FPGA and/or ASIC design and verification tasks. Access SynthWorks VHDL training courses, at: http://www.synthworks.com/vhdl_course_overview.htm

Media Contact

Jim Lewis
Director of Training
1-800-505-VHDL (8435), 503-320-0782
jim@synthworks.com
http://www.synthworks.com