OSVVM's Test Reports and Simulator Independent Scripting

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Test Reports and Scripts

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This material is derived from SynthWorks' class, VHDL Testbenches and Verification

This material is updated from time to time and the latest copy of this is available at http://www.SynthWorks.com/papers

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Test Reports and Scripts

- Agenda
  - What is OSVVM?
  - OSVVM Scripting Basics
  - OSVVM Reports
  - VHDL Code to Generate Reports
  - Managing Output Directories
  - Simplifying Code Coverage Collection

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Background

- About Jim Lewis
  - 30 years: VHDL Design and Verification
  - 20+ years: Active in IEEE VHDL WGs
  - 14 years: IEEE VHDL WG chair
  - Chief Architect of OSVVM
  - VHDL Consultant and Trainer for SynthWorks
- SynthWorks provides VHDL Training
  - Comprehensive VHDL Introduction
  - VHDL Coding for Synthesis
  - Advanced VHDL Testbenches and Verification – OSVVM Bootcamp

OSVVM is developed by the same VHDL experts who have helped develop VHDL standards. We have used our expert VHDL skills to create advanced verification capabilities.

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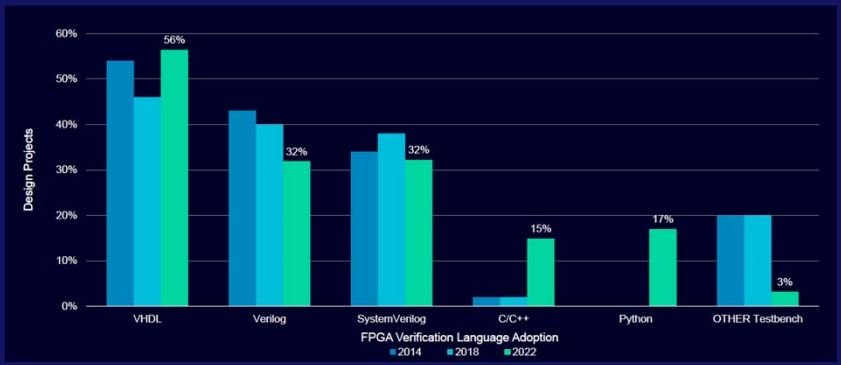
Why VHDL?

- From Wilson Research Group 2022 Functional Verification Survey
  - For FPGA design: 66% worldwide use VHDL
  - For FPGA verification: 56% worldwide use VHDL
- VHDL is #1 for FPGA Design and Verification



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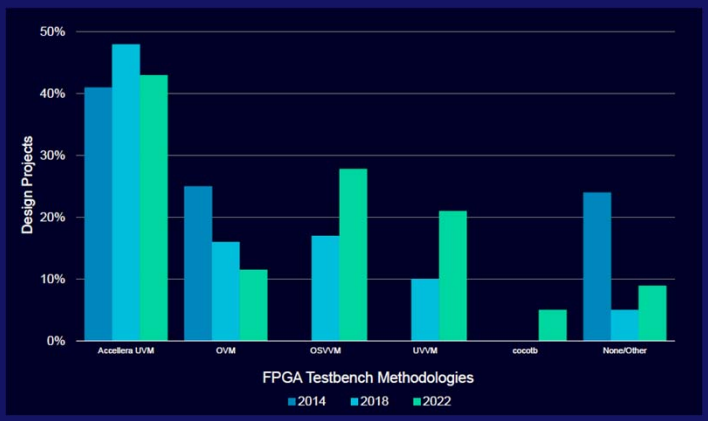
Why OSVVM?

- For FPGA Verification Libraries,
  - Worldwide: 28% use OSVVM = 50% of the VHDL FPGA users
- OSVVM is VHDL's #1 Verification Methodology



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What is OSVVM?

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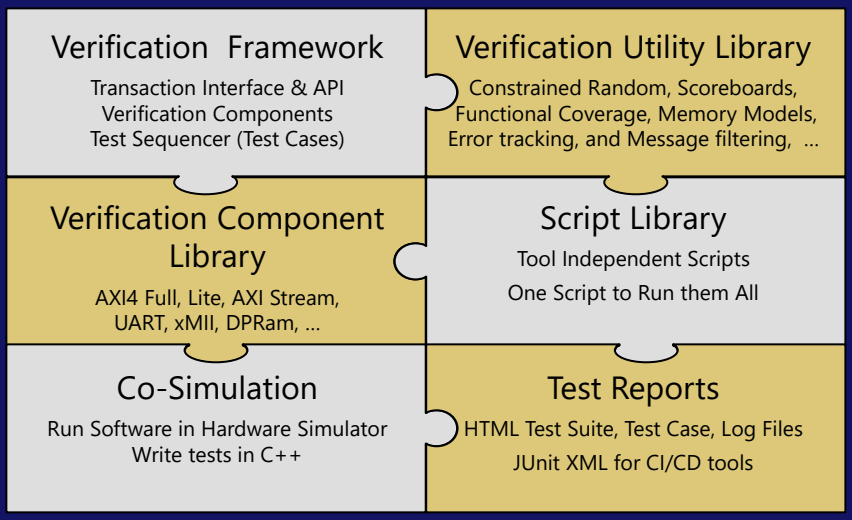

- OSVVM is Free, Open Source
- Developed by the same VHDL experts who helped with VHDL Standards

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OSVVM History

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SynthWorks Classes	1997	Transaction Framework, TbUtilPkg
	2006	RandomPkg, ResolutionPkg, ScoreboardPkg, MemoryPkg
	2010	CoveragePkg
OSVVM and SynthWorks Classes	2011	RandomPkg, CoveragePkg
	2015	AlertLogPkg, TranscriptPkg, MemoryPkg
	2016	ScoreboardGenericPkg, TbUtilPkg, ResolutionPkg
	2018	Axi4Lite, AxiStream, UART
	2020	Scripting, Specification Tracking, MIT, Virtual Interfaces, Axi4 Full and AxiStream, both with Bursting
	2021	Singleton Data Structures, HTML & JUnit XML reports
	2022	HTML Log & Scoreboard Reports, Code Coverage Reports, Ethernet VC, Arrays of Transaction Interfaces
	2023	Co-simulation of C++ Software in a Hardware Simulator AXI VC with delay randomization for xValid and xReady

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My Scripts Before OSVVM

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```
set DIR_SRC [file dirname [status file] ]
```
Source Location

```
set LIB_NAME osvvm_TbUart
if {![file isdirectory ./VHDL_LIBS/${LIB_NAME}} {
  vlib  ./VHDL_LIBS/${LIB_NAME}
}
```
Create Libraries & Map to them

```
vcom -2008 -work $LIB_NAME ${DIR_SRC}/TestCtrl_e.vhd
vcom -2008 -work $LIB_NAME ${DIR_SRC}/TbUart.vhd
vcom -2008 -work $LIB_NAME ${DIR_SRC}/TbUart_SendGet1.vhd
```
Compile

```
vsim –lib ${LIB_NAME} TbUart_SendGet1
add wave -r /TbLedFlasher/*
run 40 us
```
Simulate, add waves, & run

- Issues
  - Need help (TCL code) to find the source directory
  - Simulator Specific
  - Simulator API repeats the same information on many calls

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Why is EDA Scripting Hard?

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- Some blame TCL
- Issues
  - Simulator needs to run in a specific directory
    - Settings and Library information are in a *.ini or *.cfg
      - If not, the library info must be respecified on tool start
    - Hence, if you use "cd", you loose this information
  - Scripts need to be co-located with verification IP
    - Hence, they need directory information
  - The simulator API fundamentally misunderstands the VHDL work library
    - Work is not a name for a library
    - Work is the shorthand for the current library

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OSVVM Scripting

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```
library  osvvm_TbUart
```
Activate Library

```
analyze  ./testbench/TestCtrl_e.vhd
analyze  ./testbench/TbUart.vhd
```
Compile

```
analyze  ./testbench/TbUart_SendGet1.vhd
simulate TbUart_SendGet1
```
Simulate & Run TbUart_SendGet1

- Benefits
  - Simple, just like a list of source files …
    - … Except it is an API on top of TCL
    - Get the power of TCL without the ugly parts.
  - Settings (like current working library) are remembered
- Supports
  - GHDL and NVC (open source)
  - Siemens: Questa and ModelSim
  - Aldec: ActiveHDL and Riviera-PRO
  - Synopsys VCS, Cadence Xcelium

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Preparing to Run OSVVM Scripts

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- Create a directory named "sim" in which to run the scripts
  - Put it in the same directory as OsvvmLibraries
- Start your simulator or tclsh in the sim directory
- For RivieraPRO, GHDL (from tclsh), ModelSim, and QuestaSim:

```
source ../OsvvmLibraries/Scripts/StartUp.tcl
```

- For Active-HDL only, put the simulator in TCL mode

```
scripterconf -tcl
source ../OsvvmLibraries/Scripts/StartUp.tcl
```

- For Synopsys VCS (from tclsh):

```
source ../OsvvmLibraries/Scripts/StartVCS.tcl
```

- For Cadence Xcelium (from tclsh):

```
source ../OsvvmLibraries/Scripts/StartXcelium.tcl
```

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Calling OSVVM Scripts

- build - Call a *.pro file from command line or CI

```
build ../OsvvmLibraries/OsvvmLibraries.pro
build ../OsvvmLibraries/RunDemoTestsWithCoverage.pro
```

  - Build + EndOfTestReports generates the HTML and Junit reports

- include - Call a *.pro file from another *.pro file

```
# AXI4.pro
include ./common/common.pro
include ./Axi4Lite/Axi4Lite.pro
include ./AxiStream/AxiStream.pro
include ./Axi4/Axi4.pro
```

- Use Build and Include rather than TCL's source or EDA vendor's do
  - Used to make paths relative to directory from which the scripts run

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You don't have to like TCL

- The TCL used by OSVVM is to analyze and run test cases:

```
# Excerpt from OsvvmLibraries/osvvm/osvvm.pro
. . .
if {$::osvvm::ToolVendor eq "Aldec"}  {
  analyze VendorCovApiPkg_Aldec.vhd
} else {
  analyze VendorCovApiPkg.vhd
}
```

  - TCL uses "eq" for string equal and "ne" for string not equal

```
# Excerpt from OsvvmLibraries/OsvvmLibraries.pro
if {[DirectoryExists UART]} {
  include ./UART/UART.pro
}
```

  - DirectoryExists is from the OSVVM scripts

- Google search is enough to help you with TCL for OSVVM Scripting

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Running Test Cases

```
TestName  TbUart_SendGet1
analyze   ./testbench/TbUart_SendGet1.vhd
simulate  TbUart
```

- A test fails if the TestName name does not match the VHDL test name
- TestName is optional if its name matches the simulate name

- Abbreviation for the sequence above

```
RunTest  ./testbench/TbUart_SendGet1.vhd
```

- Design test cases so the TestName, the file name, and the simulation design unit (entity or configuration name) match

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Running Test Suites

- A Test Suite runs multiple Test Cases

```
# ./OsvvmLibraries/AXI4/AxiStream/RunAllTests.pro
TestSuite AxiStream
library osvvm_TbAxiStream

include ./testbench        ; # compile the test
include ./TestCases        ; # Run the test cases
```

- Test Cases called from above

```
# ./OsvvmLibraries/AXI4/AxiStream/TestCases/TestCases.pro
RunTest  TbStream_SendGetDemo1.vhd
RunTest  TbStream_SendGetPacketBurst1.vhd
RunTest  TbStream_MultipleDriversTransmitter1.vhd
RunTest  TbStream_MultipleDriversReceiver1.vhd
RunTest  TbStream_SendGet1.vhd
RunTest  TbStream_ByteHandling1.vhd
RunTest  TbStream_SendGetAsync1.vhd
. . .
```

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Running a Build

- A Build runs one or more test suites

```
# ./OsvvmLibraries/RunAllTests.pro
if {[DirectoryExists AXI4]} {
  include ./AXI4/RunAllTests.pro
}

if {[DirectoryExists UART]} {
  include ./UART/RunAllTests.pro
}

if {[DirectoryExists DpRam]} {
  include ./DpRam/RunAllTests.pro
}
```

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Creating OSVVM's Reports

- Reports are generated by OSVVM Scripts plus the following code:

```
-- Reference to OSVVM Utility Library
library OSVVM ;
context OSVVM.OsvvmContext ;
. . .
TestProc : process
begin
  SetTestName("TbDut") ;
  . . .
  AffirmIfEqual(Data, X"A025", "Check Data") ;
  . . .
  EndOfTestReports ;
  std.env.stop ;
end process TestProc ;
```

Name the test

Do some checks

Generate Reports
Replaces ReportAlerts

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Reports

- Build Summary Mini-Report – Text
- Build Summary Report – HTML
  - Summary of entire build
  - Summary of each test suite in the build
  - Summary of each test case within a test suite
- Test Case Reports – HTML
  - Reports on Alert, Functional Coverage, and Scoreboards
  - Links to HTML simulation transcript and test file output
- HTML'ized simulation transcript / log file (simulator output)
  - Errors shown in red
- JUnit Report – XML for Continuous Integration Tools
  - Similar to the build summary report with less information

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Build Summary Mini-Report

- When a build finishes, a single line, mini report is produced

```
BuildError: Sim_Demo FAILED,  Passed: 149,  Failed: 3,
Skipped: 0,  Analyze Errors: 0,  Simulate Errors: 0,  Build
Error Code: 0
```

  - If there are errors, this is the first place we see an indication

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Build Summary Report

Created by Scripts + EndOfTestReports

sim_RunDemoTestsWithCov Build Summary Report

Build	sim_RunDemoTestsWithCov
Status	PASSED
PASSED	31
FAILED	0
SKIPPED	0
Analyze Failures	0
Simulate Failures	0
Elapsed Time (h:m:s)	0:02:03
Elapsed Time (seconds)	123.035
Start Time	2023-07-20T20:54-0700
Simulator	RivieraPRO
Simulator Version	RivieraPRO-2022.10.117.8716
OSVVM Version	2023.07
Simulation Transcript	sim_RunDemoTestsWithCov.log
HTML Simulation Transcript	sim_RunDemoTestsWithCov_log.html
Requirements Summary	sim_RunDemoTestsWithCov_req.html
Code Coverage	Code Coverage Results
Finish Time	2023-07-20T20:56-0700

▾ sim_RunDemoTestsWithCov Test Suite Summary

TestSuites	Status	PASSED	FAILED	SKIPPED	Requirements passed / goal	Disabled Alerts	Elapsed Time
Axi4Full	PASSED	4	0	0	0 / 0	0	12.683
AxiStream	PASSED	2	0	0	0 / 0	0	6.995
Uart	PASSED	1	0	0	0 / 0	0	3.767
AlertLogPkg	PASSED	5	0	0	5 / 5	0	14.339
RandomPkg	PASSED	11	0	0	0 / 0	0	35.184
CoverageePkg_singleton	PASSED	1	0	0	0 / 0	0	3.602
MemoryPkg	PASSED	2	0	0	0 / 0	0	7.054
ScoreboardPkg_singleton	PASSED	5	0	0	0 / 0	0	19.603

▾ Axi4Full Test Case Summary

Test Case	Status	Checks			Requirements		Functional Coverage	Disabled Alerts	Elapsed Time
		Total	Passed	Failed	Goal	Passed			
TbAxi4_DemoMemoryReadWrite1	PASSED	334	334	0	0	0	43.75	0	1.616
TbAxi4_ManagerRandomTiming1	PASSED	512	512	0	0	0	100.00	0	1.657
TbAxi4_ManagerMemoryRandomTiming1	PASSED	512	512	0	0	0	100.00	0	1.679
TbAxi4_MemoryBurstPattern1	PASSED	114	114	0	0	0	100.00	0	1.421

▾ AxiStream Test Case Summary

Test Case	Status	Checks			Requirements		Functional Coverage	Disabled Alerts	Elapsed Time
		Total	Passed	Failed	Goal	Passed			
TbStream_SendGetRandom1	PASSED	1616	1616	0	0	0	100.00	0	1.469
TbStream_SendGetRandom2	PASSED	5753	5753	0	0	0	100.00	0	1.518

Build Status

- Summarizes all tests run
- Simulator & Revision
- Link to Simulation Transcript
  - Both text and html
- Link to code coverage

Test Suite Summaries

Test Suite = multiple test cases
Summarizes Pass/Fail+

Test Case Summaries

Test Case = Testbench
Identify Failing Test(s)
Links to Test Case Reports

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Build Summary Report with Errors

sim_OsvvmDemo Build Summary Report

Build	sim_OsvvmDemo
Status	FAILED
PASSED	151
FAILED	3
SKIPPED	0
Analyze Failures	0
Simulate Failures	0
Elapsed Time (h:m:s)	0:43:25
Elapsed Time (seconds)	2604.920
Start Time	2023-07-18T19:16-0700
Simulator	QuestaSim -gui
Simulator Version	QuestaSim-2022.01
OSVVM Version	2023.07
Simulation Transcript	sim_OsvvmDemo.log
HTML Simulation Transcript	sim_OsvvmDemo_log.html
Code Coverage	Code Coverage Results
Finish Time	2023-07-18T20:00-0700

▾ sim_OsvvmDemo Test Suite Summary

TestSuites	Status	PASSED	FAILED	SKIPPED	Requirements passed / goal	Disabled Alerts	Elapsed Time
Axi4Lite	PASSED	11	0	0	0 / 0	0	243.940
Axi4Full	FAILED	59	3	0	0 / 0	0	1080.200
AxiStream	PASSED	65	0	0	0 / 0	0	1029.082
Uart	PASSED	9	0	0	0 / 0	0	130.333
DpRam	PASSED	1	0	0	0 / 0	0	16.306
Ethernet	PASSED	6	0	0	0 / 0	0	74.460

▸ Axi4Lite Test Case Summary

▾ Axi4Full Test Case Summary

Test Case	Status	Checks			Requirements		Functional Coverage	Disabled Alerts	Elapsed Time
		Total	Passed	Failed	Goal	Passed			
TbAxi4_DemoMemoryReadWrite1	PASSED	334	334	0	0	0	43.75	0	16.584
TbAxi4_DemoErrorMemoryReadWrite1	FAILED	302	300	2	0	0	100.00	0	15.475
TbAxi4_BasicReadWrite	PASSED	60	60	0	0	0	100.00	0	15.103
TbAxi4_RandomReadWrite	PASSED	3000	3000	0	0	0	100.00	0	17.147
TbAxi4_RandomReadWriteByte1	PASSED	3000	3000	0	0	0	100.00	0	17.249
TbAxi4_SubordinateReadWrite1	PASSED	60	60	0	0	0	100.00	0	15.184
TbAxi4_SubordinateReadWrite2	PASSED	60	60	0	0	0	100.00	0	15.108

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Requirements Report

▾ sim_RunDemoTestsWithCov Requirement Results

Requirement	TestName	Status	Requirements		Checks			Alert Counts			Disabled Alert Counts		
			Goal	Passed	Total	Passed	Failed	Failures	Errors	Warnings	Failures	Errors	Warnings
1.1	Merged	PASSED	1	6	6	6	0	0	0	0	0	0	0
	TbAlertLog_t18_requirements	PASSED	1	1	1	1	0	0	0	0	0	0	0
	TbAlertLog_t19_requirements_print_passed	PASSED	1	1	1	1	0	0	0	0	0	0	0
	TbAlertLog_t20_requirements_explicit_hierarchy	PASSED	1	1	1	1	0	0	0	0	0	0	0
	TbAlertLog_t21_requirements_no_hierarchy	PASSED	1	1	1	1	0	0	0	0	0	0	0
	TbAlertLog_t22_requirements_w_errors	PASSED	1	1	1	1	0	0	0	0	0	0	0
	TbAlertLog_t23_read_requirements	PASSED	1	1	1	1	0	0	0	0	0	0	0
1.2	Merged	PASSED	2	12	12	12	0	0	0	0	0	0	0
	TbAlertLog_t18_requirements	PASSED	2	2	2	2	0	0	0	0	0	0	0
	TbAlertLog_t19_requirements_print_passed	PASSED	2	2	2	2	0	0	0	0	0	0	0
	TbAlertLog_t20_requirements_explicit_hierarchy	PASSED	2	2	2	2	0	0	0	0	0	0	0
	TbAlertLog_t21_requirements_no_hierarchy	PASSED	2	2	2	2	0	0	0	0	0	0	0
	TbAlertLog_t22_requirements_w_errors	PASSED	2	2	2	2	0	0	0	0	0	0	0
	TbAlertLog_t23_read_requirements	PASSED	2	2	2	2	0	0	0	0	0	0	0
1.3	Merged	FAILED	3	18	20	18	2	0	2	0	0	0	0
	TbAlertLog_t18_requirements	PASSED	3	3	3	3	0	0	0	0	0	0	0
	TbAlertLog_t19_requirements_print_passed	PASSED	3	3	3	3	0	0	0	0	0	0	0
	TbAlertLog_t20_requirements_explicit_hierarchy	PASSED	3	3	3	3	0	0	0	0	0	0	0
	TbAlertLog_t21_requirements_no_hierarchy	PASSED	3	3	3	3	0	0	0	0	0	0	0
	TbAlertLog_t22_requirements_w_errors	FAILED	3	3	5	3	2	0	2	0	0	0	0
	TbAlertLog_t23_read_requirements	PASSED	3	3	3	3	0	0	0	0	0	0	0
1.4	Merged	FAILED	4	24	26	24	2	0	2	0	0	0	0
	TbAlertLog_t18_requirements	PASSED	4	4	4	4	0	0	0	0	0	0	0
	TbAlertLog_t19_requirements_print_passed	PASSED	4	4	4	4	0	0	0	0	0	0	0
	TbAlertLog_t20_requirements_explicit_hierarchy	PASSED	4	4	4	4	0	0	0	0	0	0	0
	TbAlertLog_t21_requirements_no_hierarchy	PASSED	4	4	4	4	0	0	0	0	0	0	0
	TbAlertLog_t22_requirements_w_errors	FAILED	4	4	6	4	2	0	2	0	0	0	0
	TbAlertLog_t23_read_requirements	PASSED	4	4	4	4	0	0	0	0	0	0	0
2.1	TbAlertLog_t23_read_requirements	PASSED	2	2	2	2	0	0	0	0	0	0	0
2.2	TbAlertLog_t23_read_requirements	PASSED	2	2	2	2	0	0	0	0	0	0	0
2.3	TbAlertLog_t23_read_requirements	PASSED	2	2	2	2	0	0	0	0	0	0	0
2.4	TbAlertLog_t23_read_requirements	PASSED	2	2	2	2	0	0	0	0	0	0	0
3.1	TbAlertLog_t23_read_requirements	PASSED	1	1	1	1	0	0	0	0	0	0	0
3.2	TbAlertLog_t23_read_requirements	PASSED	1	1	1	1	0	0	0	0	0	0	0
3.3	TbAlertLog_t23_read_requirements	PASSED	1	1	1	1	0	0	0	0	0	0	0
3.4	TbAlertLog_t23_read_requirements	PASSED	1	1	1	1	0	0	0	0	0	0	0
4.1	TbAlertLog_t23_read_requirements	PASSED	1	1	1	1	0	0	0	0	0	0	0
4.2	TbAlertLog_t23_read_requirements	FAILED	2	2	4	2	2	0	2	0	0	0	0
4.3	TbAlertLog_t23_read_requirements	PASSED	3	3	3	3	0	0	0	0	0	0	0
4.4	TbAlertLog_t23_read_requirements	FAILED	4	4	5	4	1	0	1	0	0	0	0
ReqParent	TbAlertLog_t27_ID_req	FAILED	0	0	0	0	2	0	2	0	0	0	0
T1.1	Merged	PASSED	1	3	3	3	0	0	0	0	0	0	0
	TbAlertLog_t24_affirmIf_requirements	PASSED	1	1	1	1	0	0	0	0	0	0	0
	TbAlertLog_t25_read_specification	PASSED	1	1	1	1	0	0	0	0	0	0	0

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Test Case Report

TbAxi4_MemoryReadWriteDemo1 Test Case Detailed Report

Available Reports
Alert Report
Functional Coverage Report(s)
ScoreboardPkg_slv Report(s)
Link to Simulation Results
TbAxi4_MemoryReadWriteDemo1.txt
OsvvmLibraries_RunAllTestsWithCoverage Build Summary

Links

Alert Report
Functional Coverage Report
Scoreboard Reports
Simulation Results
Test Case Transcript
Link to Build Summary

TbAxi4_MemoryReadWriteDemo1 Alert Report

▸ TbAxi4_MemoryReadWriteDemo1 Alert Settings

▸ TbAxi4_MemoryReadWriteDemo1 Alert Results

Alert Report

Settings (hidden)
Results (hidden)

TbAxi4_MemoryReadWriteDemo1 Coverage Report

Total Coverage: 43.75

▸ Cov1 Coverage Model Coverage: 37.5
▸ Cov2 Coverage Model Coverage: 37.5
▸ Cov1b Coverage Model Coverage: 50.0
▸ Cov2b Coverage Model Coverage: 50.0

Functional Coverage Report

Report for each FC model in testbench (each hidden)

TbAxi4_MemoryReadWriteDemo1 Scoreboard Report for Scoreboard_slv

Name	ParentName	ItemCount	ErrorCount	ItemsChecked	ItemsPopped	ItemsDropped	FifoCount
WriteAddressFIFO	memory_1	40	0	0	40	0	0
WriteDataFifo	memory_1	150	0	0	150	0	0
WriteResponseFifo	memory_1	40	0	0	40	0	0
ReadAddressFifo	memory_1	40	0	0	40	0	0
ReadDataFifo	memory_1	150	0	0	150	0	0
WriteResponse Scoreboard	manager_1	40	0	40	40	0	0
ReadResponse Scoreboard	manager_1	150	0	150	150	0	0
WriteAddressFIFO	manager_1	40	0	0	40	0	0
WriteDataFifo	manager_1	150	0	0	150	0	0
ReadAddressFifo	manager_1	40	0	0	40	0	0

Scoreboard Report

One Table for each Scoreboard type.
One row in table for each scoreboard.

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Test Case Report: Alert Report

TbAxi4_RandomReadWrite Alert Report

▾ TbAxi4_RandomReadWrite Alert Settings

Setting		Value	Description
FailOnWarning		true	If true, warnings are a test error
FailOnDisabledErrors		true	If true, Disabled Alert Counts are a test error
FailOnRequirementErrors		true	If true, Requirements Errors are a test error
External	Failures	0	Added to Alert Counts in determine total errors
	Errors	0	
	Warnings	0	
Expected	Failures	0	Subtracted from Alert Counts in determine total errors
	Errors	0	
	Warnings	0	

Alert Settings

▾ TbAxi4_RandomReadWrite Alert Results

Name	Status	Checks			Requirements		Alert Counts			Disabled Alert Counts		
		Total	Passed	Failed	Goal	Passed	Failures	Errors	Warnings	Failures	Errors	Warnings
TbAxi4_RandomReadWrite	PASSED	3000	3000	0	0	0	0	0	0	0	0	0
Default	PASSED	1750	1750	0	0	0	0	0	0	0	0	0
OSVVM	PASSED	0	0	0	0	0	0	0	0	0	0	0
subordinate_1	PASSED	0	0	0	0	0	0	0	0	0	0	0
Protocol Error	PASSED	0	0	0	0	0	0	0	0	0	0	0
Data Check	PASSED	0	0	0	0	0	0	0	0	0	0	0
No response	PASSED	0	0	0	0	0	0	0	0	0	0	0
interrupthandler_1	PASSED	0	0	0	0	0	0	0	0	0	0	0
WriteBurstFifo	PASSED	0	0	0	0	0	0	0	0	0	0	0
ReadBurstFifo	PASSED	0	0	0	0	0	0	0	0	0	0	0
manager_1	PASSED	0	0	0	0	0	0	0	0	0	0	0
Protocol Error	PASSED	0	0	0	0	0	0	0	0	0	0	0
Data Check	PASSED	250	250	0	0	0	0	0	0	0	0	0
No response	PASSED	0	0	0	0	0	0	0	0	0	0	0
WriteResponse Scoreboard	PASSED	500	500	0	0	0	0	0	0	0	0	0
ReadResponse Scoreboard	PASSED	500	500	0	0	0	0	0	0	0	0	0
WriteBurstFifo	PASSED	0	0	0	0	0	0	0	0	0	0	0
ReadBurstFifo	PASSED	0	0	0	0	0	0	0	0	0	0	0

Alert Report

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Test Case Report: Alert Report with Errors

TbAxi4_DemoErrorMemoryReadWrite1 Alert Report

▾ TbAxi4_DemoErrorMemoryReadWrite1 Alert Settings

Setting		Value	Description
FailOnWarning		true	If true, warnings are a test error
FailOnDisabledErrors		true	If true, Disabled Alert Counts are a test error
FailOnRequirementErrors		true	If true, Requirements Errors are a test error
External	Failures	0	Added to Alert Counts in determine total errors
	Errors	0	
	Warnings	0	
Expected	Failures	0	Subtracted from Alert Counts in determine total errors
	Errors	0	
	Warnings	0	

Status FAILED in table indicates

- TbAxi4_DemoErrorMemoryReadWrite1 has 2 errors
- The 2 errors were detected in the manager_1 VC
- One error is in the manager_1::Data Check
- One error is in manager1::ReadBurstFifo

▾ TbAxi4_DemoErrorMemoryReadWrite1 Alert Results

Name	Status	Checks			Requirements		Alert Counts			Disabled Alert Counts		
		Total	Passed	Failed	Goal	Passed	Failures	Errors	Warnings	Failures	Errors	Warnings
TbAxi4_DemoErrorMemoryReadWrite1	FAILED	302	300	2	0	0	0	2	0	0	0	0
Default	PASSED	0	0	0	0	0	0	0	0	0	0	0
OSVVM	PASSED	0	0	0	0	0	0	0	0	0	0	0
Testbench	PASSED	20	20	0	0	0	0	0	0	0	0	0
manager_1	FAILED	0	0	2	0	0	0	2	0	0	0	0
Protocol Error	PASSED	0	0	0	0	0	0	0	0	0	0	0
Data Check	FAILED	16	15	1	0	0	0	1	0	0	0	0
No response	PASSED	0	0	0	0	0	0	0	0	0	0	0
WriteResponse Scoreboard	PASSED	40	40	0	0	0	0	0	0	0	0	0
ReadResponse Scoreboard	PASSED	134	134	0	0	0	0	0	0	0	0	0
WriteBurstFifo	PASSED	0	0	0	0	0	0	0	0	0	0	0
ReadBurstFifo	FAILED	92	91	1	0	0	0	1	0	0	0	0
memory_1	PASSED	0	0	0	0	0	0	0	0	0	0	0
No response	PASSED	0	0	0	0	0	0	0	0	0	0	0
Data Check	PASSED	0	0	0	0	0	0	0	0	0	0	0
memory_1:memory	PASSED	0	0	0	0	0	0	0	0	0	0	0
WriteBurstFifo	PASSED	0	0	0	0	0	0	0	0	0	0	0
ReadBurstFifo	PASSED	0	0	0	0	0	0	0	0	0	0	0

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Test Case Report: Functional Coverage

Uart7_Random_part3 Coverage Report

Total Coverage: 100.00

▼ UART_RX_STIM_COV Coverage Model **Coverage: 100.0**

▼ UART_RX_STIM_COV Coverage Settings

CovWeight	1
Goal	100.0
WeightMode	at_least
Seeds	824213985 792842968
CountMode	count_first
IllegalMode	illegal_on
Threashold	45.0
ThresholdEnable	0
TotalCovCount	100
TotalCovGoal	100

Coverage Model Settings

▼ UART_RX_STIM_COV Coverage Bins

Name	Type	Mode	Data	Idle	Count	AtLeast	Percent Coverage
NORMAL	Count	1 to 1	0 to 255	0 to 0	63	63	100.0
NORMAL	Count	1 to 1	0 to 255	1 to 15	7	7	100.0
PARITY	Count	3 to 3	0 to 255	2 to 15	11	11	100.0
STOP	Count	5 to 5	1 to 255	2 to 15	11	11	100.0
PARITY_STOP	Count	7 to 7	1 to 255	2 to 15	6	6	100.0
BREAK	Count	9 to 15	11 to 30	2 to 15	2	2	100.0
Total Percent Coverage:	100.0						

Coverage Results

▼ UART_RX_COV Coverage Model **Coverage: 100.0**

▶ UART_RX_COV Coverage Settings

▼ UART_RX_COV Coverage Bins

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Test Case Report: Scoreboards

TbAxi4_DemoErrorMemoryReadWrite1 Scoreboard Report for Scoreboard_slv

Name	ParentName	ItemCount	ErrorCount	ItemsChecked	ItemsPopped	ItemsDropped	FifoCount
WriteResponse Scoreboard	manager_1	40	0	40	40	0	0
ReadResponse Scoreboard	manager_1	134	0	134	134	0	0
WriteAddressFIFO	manager_1	40	0	0	40	0	0
WriteDataFifo	manager_1	134	0	0	134	0	0
ReadAddressFifo	manager_1	40	0	0	40	0	0
ReadAddressTransactionFifo	manager_1	40	0	0	40	0	0
ReadDataFifo	manager_1	134	0	0	134	0	0
WriteAddressFIFO	memory_1	40	0	0	40	0	0
WriteDataFifo	memory_1	134	0	0	134	0	0
WriteResponseFifo	memory_1	40	0	0	40	0	0
ReadAddressFifo	memory_1	40	0	0	40	0	0
ReadDataFifo	memory_1	134	0	0	134	0	0
WriteBurstFifo	manager_1	102	0	0	102	0	0
ReadBurstFifo	manager_1	102	1	92	102	0	0

- A separate table is created for each scoreboard instance
- Each row in the table has statistics for a single scoreboard

- Tables for Scoreboard_slv and Scoreboard_int are automatically generated
- Use WriteScoreboardYaml to generate reports for user created scoreboards

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HTML'ized Simulation Transcript

Simulation Transcript

- Details are hidden
- Rotate triangle to see details
- Scan a file that is otherwise 100K+ lines in seconds

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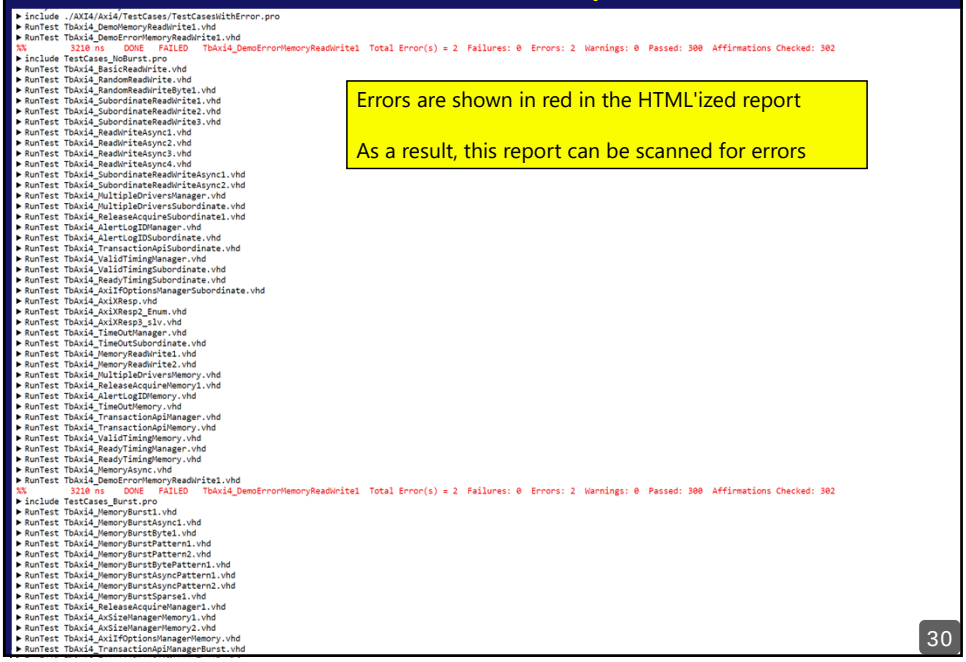
SynthWorks

HTML'ized Simulation Transcript with Errors



Errors are shown in red in the HTML'ized report

As a result, this report can be scanned for errors

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HTML'ized Simulation Transcript – Test Case Information

SynthWorks

```
▶ RunTest TbAxi4_AxiXResp.vhd
▶ include ./Axi4/RunAllTests.pro
▶ TestSuite Axi4Full
▶ library osvvm_TbAxi4 C:/tools/sim_temp/RivieraPRO-2022.04.117.8517
▶ include ./testbench
▶ library osvvm_TbAxi4 C:/tools/sim_temp/RivieraPRO-2022.04.117.8517
▶ analyze ../TestCases/OsvvmTestCommonPkg.vhd
▶ analyze TestCtrl_e.vhd
▶ analyze TbAxi4.vhd
▶ analyze TbAxi4Memory.vhd
▶ include ./TestCases
▼ RunTest TbAxi4_MemoryReadWriteDemo1.vhd

#
# analyze TbAxi4_MemoryReadWriteDemo1.vhd
# vcom {*}-2008 -relax -work osvvm_TbAxi4 ../../OsvvmLibraries/AXI4/Axi4/TestCases/TbAxi4_MemoryReadWriteDemo1.vhd
# ACOM: Warning: DAGGEN_0523: The source is compiled without the -dbg switch. Line breakpoints and assertion debug will not be available.
# ACOM: File: ../../OsvvmLibraries/AXI4/Axi4/TestCases/TbAxi4_MemoryReadWriteDemo1.vhd
# ACOM: Compile Architecture "MemoryReadWriteDemo1" of Entity "TestCtrl"
# ACOM: Compile Configuration "TbAxi4_MemoryReadWriteDemo1"
# ACOM: Compile success 0 Errors 0 Warnings  Analysis time :  0.1 [s]
# ACDB: Closing Code Coverage session.
# VSIM: Simulation has finished.
# simulate TbAxi4_MemoryReadWriteDemo1
#

# Simulate Start time 17:12:02
# vsim {*}-acdb_cov sbm -cc_all -t ps -lib osvvm_TbAxi4 TbAxi4_MemoryReadWriteDemo1
# ELBREAD: Elaboration process.
# ELBREAD: Elaboration time 0.0 [s].
# KERNEL: Main thread initiated.
# KERNEL: Kernel process initialization phase.
# ELAB2: Elaboration final pass...
# KERNEL: PLI/VHPI kernel's engine initialization done.
# PLI: Loading library 'C:\tools\Aldec\Riviera-PRO-2022.04-x64\bin\systf.dll'
# VHPI: Loading library 'systf.dll'
# ELAB2: Create instances ...
# KERNEL: Time resolution set to 1ps.
# ELAB2: Create instances complete.
# SLP: Started
# SLP: Elaboration phase ...
# SLP: Elaboration phase ... skipped, nothing to simulate in SLP mode : 0.0 [s]
# SLP: Finished : 0.0 [s]
# ELAB2: Elaboration final pass complete - time: 0.1 [s].
# ACDB: Code Coverage session started in hierarchical mode for all units.
# KERNEL: Kernel process initialization done.
# Allocation: Simulator allocated 44785 kB (elbread=427 elab2=11108 kernel=33249 sdf=0)
# KERNEL: ASDB file was created in location C:/SynthWorks/Dev/_osvvm/_sim/riviera/dataset.asdb
# VSIM: 87 object(s) traced.
# KERNEL: %% Log    PASSED  in Default, Default BurstMode is ADDRESS_BUS_BURST_WORD_MODE 0 at 110 ns
# KERNEL: %% Log    PASSED  in Default, BurstMode Received : 0 at 110 ns
# KERNEL: %% Log    ALWAYS  in Default, Write and Read. Addr = 0000.  16 words at 110 ns
# KERNEL: %% Log    INFO    in manager_1, Write Data.  WData: 00000001  WStrb: 1111  Operation# 1 at 110 ns
# KERNEL: %% Log    INFO    in manager_1, Write Address.  AWAddr: 00000010  AWProt: 000  Operation# 1 at 110 ns
# KERNEL: %% Log    DEBUG   in manager_1, Waiting for Write Response  at 110 ns
```

Simulation Transcript

When viewed from Test Case Report, it jumps to the simulation's results

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HTML'ized Simulation Transcript – Test Case Information

SynthWorks

```
▶ RunTest TbAxi4_WriteOptions.vhd
▶ RunTest TbAxi4_MemoryReadWrite1.vhd
▶ RunTest TbAxi4_AxiXResp.vhd
▶ RunTest TbAxi4_AxiXResp2_Enum.vhd
▶ TestSuite Axi4Full
▶ include ./AXI4/Axi4/testbench
▶ analyze ../TestCases/OsvvmTestCommonPkg.vhd
▼ analyze TestCtrl_e.vhd

▶ analyze TbAxi4.vhd
▶ analyze TbAxi4Memory.vhd
▶ include ./AXI4/Axi4/TestCases/TestCasesWithError.pro
▶ RunTest TbAxi4_DemoMemoryReadWrite1.vhd
▼ RunTest TbAxi4_DemoErrorMemoryReadWrite1.vhd

TestName TbAxi4_DemoErrorMemoryReadWrite1
analyze TbAxi4_DemoErrorMemoryReadWrite1.vhd
End time: 16:24:28 on May 07,2023, Elapsed time: 0:00:15
Errors: 0, Warnings: 0
Simulation Start time 16:24:28
simulate TbAxi4_DemoErrorMemoryReadWrite1
vsim -t ps -lib osvvm_TbAxi4 TbAxi4_DemoErrorMemoryReadWrite1 -quiet -coverage -suppress 8683 -suppress 8684
Start time: 16:24:28 on May 07,2023
** Note: (vsim-8009) Loading existing optimized design _opt
%%          110 ns    Log     PASSED     in Testbench,                    Default BurstMode is ADDRESS_BUS_BURST_WORD_MODE 0
%%          110 ns    Log     PASSED     in Testbench,                    BurstMode Received : 0
%%          110 ns    Log     ALWAYS     in Testbench,                    Write and Read. Addr = 0000.  16 words
%%          110 ns    Log     INFO       in manager_1,                    Write Address.  AWAddr: 00000010  AWProt: 000  Operation# 1
%%          110 ns    Log     INFO       in manager_1,                    Write Data.  WData: 00000001  WStrb: 1111  Operation# 1

. . .

%%         1030 ns    Log     INFO       in manager_1,                    Read Address.  ARAddr: 000010F0  ARProt: 000  Operation# 31
%%         1040 ns    Log     INFO       in memory_1,                     Memory Read.  ARAddr: 000010F0  ARProt: 000  RData: 0000100F  Operation# 30
%%         1050 ns    Log     PASSED     in manager_1: ReadResponse Scoreboard,    Received: 0   Item Number: 31
%%         1050 ns    Log     PASSED     in manager_1: Data Check,        Read Data: 0000100F  Read Address: 000010F0  Prot: 0
%%         1050 ns    Log     INFO       in manager_1,                    Read Address.  ARAddr: 000010F0  ARProt: 000  Operation# 32
%%         1060 ns    Log     INFO       in memory_1,                     Memory Read.  ARAddr: 000010F0  ARProt: 000  RData: 0000100F  Operation# 31
%%         1070 ns    Log     PASSED     in manager_1: ReadResponse Scoreboard,    Received: 0   Item Number: 32
%%         1070 ns    Alert   ERROR      in manager_1: Data Check,        Read Data: 0000100F  Read Address: 000010F0  Prot: 0   Expected: 00001010
%%         1070 ns    Log     ALWAYS     in Default,                      WriteBurst and ReadBurst.  Addr = 2000.  16 words
%%         1070 ns    Log     INFO       in manager_1,                    Write Address.  AWAddr: 00002000  AWProt: 000  Operation# 33
%%         1070 ns    Log     INFO       in manager_1,                    Write Data.  WData: 00002001  WStrb: 1111  Operation# 33
%%         1080 ns    Log     INFO       in memory_1,                     Memory Write.  AWAddr: 00002000  AWProt: 000  WData: 00002001  WStrb: 1111  Operation# 32

. . .

%%         1400 ns    Log     PASSED     in manager_1: ReadBurstFifo,        Received: 0000200D   Item Number: 13
%%         1400 ns    Log     PASSED     in manager_1: ReadBurstFifo,        Received: 0000200E   Item Number: 14
%%         1400 ns    Log     PASSED     in manager_1: ReadBurstFifo,        Received: 0000200F   Item Number: 15
%%         1400 ns    Alert   ERROR      in manager_1: ReadBurstFifo,        Received: 00002010   Expected: 00002011   Item Number: 16
%%         1400 ns    Log     ALWAYS     in Testbench,                    Burst Vector.  Addr = 3000, 13 Words -- unaligned
%%         1400 ns    Log     INFO       in manager_1,                    Write Address.  AWAddr: 00003000  AWProt: 000  Operation# 34
%%         1400 ns    Log     INFO       in manager_1,                    Write Data.  WData: 0001UUUU  WStrb: 1100  Operation# 49
%%         1410 ns    Log     INFO       in memory_1,                     Memory Write.  AWAddr: 00003000  AWProt: 000  WData: 0001UUUU  WStrb: 1100  Operation
%%         1410 ns    Log     INFO       in manager_1,                    Write Data.  WData: 00000003  WStrb: 1111  Operation# 50
%%         1420 ns    Log     INFO       in manager_1,                    Write Data.  WData: 00000005  WStrb: 1111  Operation# 51
```

Simulation Transcript

When viewed from Test Case Report, it jumps to the simulation's results

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HTML'ized Simulation Transcript – Test Case Information

SynthWorks

```
▶ RunTest TbAxi4_WriteOptions.vhd
▶ RunTest TbAxi4_MemoryReadWrite1.vhd
▶ RunTest TbAxi4_AxiXResp.vhd
▶ RunTest TbAxi4_AxiXResp2_Enum.vhd
▶ TestSuite Axi4Full
▶ include ./AXI4/Axi4/testbench
▶ analyze ../TestCases/OsvvmTestCommonPkg.vhd
▼ analyze TestCtrl_e.vhd

▶ analyze TbAxi4.vhd
▶ analyze TbAxi4Memory.vhd
▶ include ./AXI4/Axi4/TestCases/TestCasesWithError.pro
▶ RunTest TbAxi4_DemoMemoryReadWrite1.vhd
▼ RunTest TbAxi4_DemoErrorMemoryReadWrite1.vhd

TestName TbAxi4_DemoErrorMemoryReadWrite1
analyze TbAxi4_DemoErrorMemoryReadWrite1.vhd
End time: 16:24:28 on May 07,2023, Elapsed time: 0:00:15
Errors: 0, Warnings: 0
Simulation Start time 16:24:28
simulate TbAxi4_DemoErrorMemoryReadWrite1
vsim -t ps -lib osvvm_TbAxi4 TbAxi4_DemoErrorMemoryReadWrite1 -quiet -coverage -suppress 8683 -suppress 8684
Start time: 16:24:28 on May 07,2023
** Note: (vsim-8009) Loading existing optimized design _opt
%%         110 ns    Log     PASSED    in Testbench,                          Default BurstMode is ADDRESS_BUS_BURST_WORD_MODE 0
%%         110 ns    Log     PASSED    in Testbench,                          BurstMode Received : 0
%%         110 ns    Log     ALWAYS    in Testbench,                          Write and Read. Addr = 0000.  16 words
%%         110 ns    Log     INFO      in manager_1,                          Write Address.  AWAddr: 00000010  AWProt: 000  Operation# 1
%%         110 ns    Log     INFO      in manager_1,                          Write Data.  WData: 00000001  WStrb: 1111  Operation# 1

. . .

%%        1030 ns    Log     INFO      in manager_1,                          Read Address.  ARAddr: 000010F0  ARProt: 000  Operation# 31
%%        1040 ns    Log     INFO      in memory_1,                           Memory Read.  ARAddr: 000010F0  ARProt: 000  RData: 0000100F  Operation# 30
%%        1050 ns    Log     PASSED    in manager_1: ReadResponse Scoreboard,    Received: 0   Item Number: 31
%%        1050 ns    Log     PASSED    in manager_1: Data Check,              Read Data: 0000100F  Read Address: 000010F0  Prot: 0
%%        1050 ns    Log     INFO      in manager_1,                          Read Address.  ARAddr: 000010F0  ARProt: 000  Operation# 32
%%        1060 ns    Log     INFO      in memory_1,                           Memory Read.  ARAddr: 000010F0  ARProt: 000  RData: 0000100F  Operation# 31
%%        1070 ns    Log     PASSED    in manager_1: ReadResponse Scoreboard,    Received: 0   Item Number: 32
%%        1070 ns    Alert   ERROR     in manager_1: Data Check,              Read Data: 0000100F  Read Address: 000010F0  Prot: 0   Expected: 00001010
%%        1070 ns    Log     ALWAYS    in Default,                            WriteBurst and ReadBurst.  Addr = 2000.  16 words
%%        1070 ns    Log     INFO      in manager_1,                          Write Address.  AWAddr: 00002000  AWProt: 000  Operation# 33
%%        1070 ns    Log     INFO      in manager_1,                          Write Data.  WData: 00002001  WStrb: 1111  Operation# 33
%%        1080 ns    Log     INFO      in memory_1,                           Memory Write.  AWAddr: 00002000  AWProt: 000  WData: 00002001  WStrb: 1111  Operation# 32

. . .

%%        1400 ns    Log     PASSED    in manager_1: ReadBurstFifo,              Received: 0000200D   Item Number: 13
%%        1400 ns    Log     PASSED    in manager_1: ReadBurstFifo,              Received: 0000200E   Item Number: 14
%%        1400 ns    Log     PASSED    in manager_1: ReadBurstFifo,              Received: 0000200F   Item Number: 15
%%        1400 ns    Alert   ERROR     in manager_1: ReadBurstFifo,              Received: 00002010   Expected: 00002011   Item Number: 16
%%        1400 ns    Log     ALWAYS    in Testbench,                          Burst Vector.  Addr = 3000, 13 Words -- unaligned
%%        1400 ns    Log     INFO      in manager_1,                          Write Address.  AWAddr: 00003000  AWProt: 000  Operation# 34
%%        1400 ns    Log     INFO      in manager_1,                          Write Data.  WData: 0001UUUU  WStrb: 1100  Operation# 49
%%        1410 ns    Log     INFO      in memory_1,                           Memory Write.  AWAddr: 00003000  AWProt: 000  WData: 0001UUUU  WStrb: 1100  Operation# 33
%%        1410 ns    Log     INFO      in manager_1,                          Write Data.  WData: 00000003  WStrb: 1111  Operation# 50
%%        1420 ns    Log     INFO      in manager_1,                          Write Data.  WData: 00000005  WStrb: 1111  Operation# 51
```

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VHDL Transcript File

SynthWorks

```
% Log    ALWAYS   in Default, Transmit 16 bytes.  Cover Random at 110 ns
% Log    INFO     in transmitter_1, Axi Stream Send.  TData: 63200124  TStrb: 1111  TKeep: 1111  TID: 01  TDest: 2  TUser: 3  TLast: 0  Operation# 1 at 110 ns
% Log    INFO     in transmitter_1, Axi Stream Send.  TData: 05022122  TStrb: 1111  TKeep: 1111  TID: 01  TDest: 2  TUser: 3  TLast: 0  Operation# 2 at 120 ns
% Log    INFO     in transmitter_1, Axi Stream Send.  TData: 41072646  TStrb: 1111  TKeep: 1111  TID: 01  TDest: 2  TUser: 3  TLast: 0  Operation# 3 at 130 ns
% Log    INFO     in transmitter_1, Axi Stream Send.  TData: 00276162  TStrb: 1111  TKeep: 1111  TID: 01  TDest: 2  TUser: 3  TLast: 1  Operation# 4 at 140 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 24   Item Number: 1 at 150 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 01   Item Number: 2 at 150 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 20   Item Number: 3 at 150 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 63   Item Number: 4 at 150 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 22   Item Number: 5 at 150 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 21   Item Number: 6 at 150 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 02   Item Number: 7 at 150 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 05   Item Number: 8 at 150 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 46   Item Number: 9 at 150 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 26   Item Number: 10 at 150 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 07   Item Number: 11 at 150 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 41   Item Number: 12 at 150 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 62   Item Number: 13 at 150 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 61   Item Number: 14 at 150 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 27   Item Number: 15 at 150 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 00   Item Number: 16 at 150 ns
% Log    INFO     in receiver_1, Burst Check.  Operation# 1  Last Data: 00276162  TID: 01  TDest: 2  TUser: 3  TLast: 1 at 150 ns
% Log    PASSED   in receiver_1, Burst Check WordCount Received : 16 at 150 ns
% Log    PASSED   in receiver_1, ID Received : 01 at 150 ns
% Log    PASSED   in receiver_1, DEST Received : 2 at 150 ns
% Log    PASSED   in receiver_1, USER Received : 3 at 150 ns
% Log    PASSED   in receiver_1, Last Received : 1 at 150 ns
% Log    ALWAYS   in Default, Transmit 14 bytes. at 190 ns
% Log    INFO     in transmitter_1, Axi Stream Send.  TData: 04230664  TStrb: 1111  TKeep: 1111  TID: 02  TDest: 3  TUser: 4  TLast: 0  Operation# 5 at 190 ns
% Log    INFO     in transmitter_1, Axi Stream Send.  TData: 67604742  TStrb: 1111  TKeep: 1111  TID: 02  TDest: 3  TUser: 4  TLast: 0  Operation# 6 at 200 ns
% Log    INFO     in transmitter_1, Axi Stream Send.  TData: 45034465  TStrb: 1111  TKeep: 1111  TID: 02  TDest: 3  TUser: 4  TLast: 0  Operation# 7 at 210 ns
% Log    INFO     in transmitter_1, Axi Stream Send.  TData: XXXX4366  TStrb: 0011  TKeep: 0011  TID: 02  TDest: 3  TUser: 4  TLast: 1  Operation# 8 at 220 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 64   Item Number: 17 at 230 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 06   Item Number: 18 at 230 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 23   Item Number: 19 at 230 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 04   Item Number: 20 at 230 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 42   Item Number: 21 at 230 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 47   Item Number: 22 at 230 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 60   Item Number: 23 at 230 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 67   Item Number: 24 at 230 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 65   Item Number: 25 at 230 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 44   Item Number: 26 at 230 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 03   Item Number: 27 at 230 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 45   Item Number: 28 at 230 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 66   Item Number: 29 at 230 ns
% Log    PASSED   in receiver_1: RxBurstFifo,    Received: 43   Item Number: 30 at 230 ns
% Log    INFO     in receiver_1, Burst Check.  Operation# 2  Last Data: ----4366  TID: 02  TDest: 3  TUser: 4  TLast: 1 at 230 ns
% Log    PASSED   in receiver_1, Burst Check WordCount Received : 14 at 230 ns
% Log    PASSED   in receiver_1, ID Received : 02 at 230 ns
% Log    PASSED   in receiver_1, DEST Received : 3 at 230 ns
% Log    PASSED   in receiver_1, USER Received : 4 at 230 ns
% Log    PASSED   in receiver_1, Last Received : 1 at 230 ns
% Log    ALWAYS   in Default, Transmit 17 bytes. at 230 ns
% Log    INFO     in transmitter_1, Axi Stream Send.  TData: 67234025  TStrb: 1111  TKeep: 1111  TID: 03  TDest: 4  TUser: 5  TLast: 0  Operation# 9 at 2
% Log    INFO     in transmitter_1, Axi Stream Send.  TData: 20454520  TStrb: 1111  TKeep: 1111  TID: 03  TDest: 4  TUser: 5  TLast: 0  Operation# 10 at
```

Created by TranscriptOpen
Test Case Report links to this file

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Skipping Tests

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- For GHDL, we need to skip tests that use external names
- SkipTest allows tracking of why some tests were not run

```
if {$::osvvm::ToolVendor eq "GHDL"} {
  SkipTest TbResolution_Array_1  "Not for GHDL"
} else {
  RunTest   TbResolutionPkg_Array_1.vhd
}
```

- Skipped tests are tracked in the build summary report

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Managing OSVVM Output Directories

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```
# OsvvmLibraries/Scripts/LocalScriptDefaults.tcl – user created
namespace eval ::osvvm {
  # Directory for all Ouput
  variable OutputBaseDirectory        ""

  # Directory for logs
  # ToolNameVersion = <ToolName>-<Version>
  variable LogSubdirectory            "logs/${ToolNameVersion}"

  # Directory for Reports (Test Case *.html)
  variable ReportsSubdirectory        "reports"

  # Directory for Reports (VHDL Code generated)
  variable ResultsSubdirectory        "results"

  # VHDL Library Directories
  variable VhdlLibraryParentDirectory ""
  variable VhdlLibraryDirectory       "VHDL_LIBS"
  variable VhdlLibrarySubdirectory    "${ToolNameVersion}"

  # Code Coverage Directory
  variable CoverageSubdirectory       "CodeCoverage"
}
```

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Where are the Reports?

- Build Summary
  - ${OutputBaseDirectory}/<Directory>_<ScriptName>.html
  - OsvvmLibraries_RunAllTests.html
- Test Case Reports
  - ${ReportsSubdirectory}/<TestSuiteName>/<TestCase>.html
- Results written by TranscriptOpen
  - OSVVM moves files to directory:
    - ${ResultsSubdirectory} /<TestSuiteName>/<TestFileName>
- Simulator Transcripts – aka logs
  - ${LogSubdirectory}/<Directory>_<ScriptName>.html
  - OsvvmLibraries_RunAllTests.html

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Code Coverage Support

- Enable coverage at a layer above the analyze and simulate scripts

```
# OsvvmLibraries/RunAllTestsWithCoverage.pro - similar
SetCoverageAnalyzeEnable true
SetCoverageSimulateEnable true

include OsvvmLibraries.pro

SetCoverageAnalyzeEnable false

include RunAllTests.pro

SetCoverageSimulateEnable false
```

Turn on Coverage

Turn off Analyze Coverage

Turn off Simulate Coverage

- Each test case produces a coverage database.
- Merge coverage for each test case into test suite coverage.
- Merge coverage for each test suite into the build coverage.
- Create HTML coverage report for the build.

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Code Coverage Support

- By default, OSVVM collects coverage for
  - Statement, branch, and statemachine

```
SetCoverageAnalyzeOptions "-coverage sbm"

SetCoverageSimulateOptions "-acdb_cov sbm -cc_all"
```

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Working with Project Libraries

- Compile OSVVM libraries into a shared project location

```
SetLibraryDirectory C:/tools/sim_temp/OSVVM

build ../OsvvmLibraries/OsvvmLibraries.pro

SetLibraryDirectory ""
```

- Each project would then link in the OSVVM libraries

```
LinkLibraryDirectory C:/tools/sim_temp/OSVVM
```

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Other Settings

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```
SetVHDLVersion          "2008"    ;# Values 1993, 2002, 2008, 2019

SetSimulatorResolution "ps"       ;#

SetTranscriptType       "html"    ;# html log
```

```
SetVhdlAnalyzeOptions       ""

SetVerilogAnalyzeOptions    ""

SetExtendedAnalyzeOptions   ""

SetExtendedSimulateOptions ""
```

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Getting OSVVM & Running Scripts

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- Get the sources:

```
git clone --recursive https://github.com/osvvm/OsvvmLibraries
```

  - Alternately, a zip file is at: osvvm.org/downloads

- Initialize the simulator – see Documentation/Scripts_user_guide.pdf

```
file mkdir sim ;   # In directory containing OsvvmLibraries
cd   sim
source ../OsvvmLibraries/Scripts/StartUp.tcl
```

- Build all OSVVM and Run All VC Tests

```
build $OsvvmLibraries/OsvvmLibraries.pro
build $OsvvmLibraries/RunAllTests.pro
```

  - Each VC has a RunAllTests and RunDemoTests

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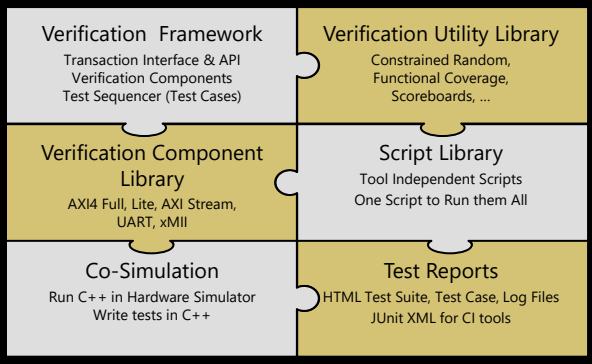
All you need is ... OSVVM



- Benefits
  - Simple scripts that run most simulators
  - The scripts are TCL, however, TCL is rarely used
  - HTML Build Reports summarizing all tests run
  - HTML Test Case Reports with details on errors, FC, and SB for each test
  - JUnit XML Reports for Continuous Integration tools (CI)
  - Simplify Code Coverage Collection

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SynthWorks VHDL Classes

Comprehensive VHDL Introduction 4 Days - beginners class
http://www.synthworks.com/comprehensive_vhdl_introduction.htm
A design and verification engineer's introduction to VHDL syntax, RTL coding, and testbenches. Students get VHDL hardware experience with our FPGA based lab board.

Advanced VHDL Testbenches and Verification - OSVVM Boot Camp - 5 days
http://www.synthworks.com/vhdl_testbench_verification.htm
Learn the latest VHDL verification techniques including transaction based modeling, self-checking, scoreboards, memory modeling, functional coverage, directed, algorithmic, constrained random, and intelligent testbench test generation. Create a VHDL testbench environment that is competitive with other verification languages, such as SystemVerilog or 'e'. Our techniques work on VHDL simulators without additional licenses and are accessible to RTL engineers.

VHDL Coding for Synthesis 4 Days
http://www.synthworks.com/vhdl_rtl_synthesis.htm
Learn VHDL RTL (FPGA and ASIC) coding styles, methodologies, design techniques, problem solving techniques, and advanced language constructs to produce better, faster, and smaller logic.

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OSVVM Resources

- Documentation
  - HTML: https://osvvm.github.io/Overview/Osvvm1About.html
  - PDF: OsvvmLibraries/Documentation - in OSVVM release
- Forum: https://osvvm.org
- Recorded Webinars
  - OSVVM: Leading Edge Verification for the VHDL Community
    - https://www.youtube.com/watch?v=KVmGDy_PHNI
  - Faster than Lite Verification Component Development with OSVVM
    - https://www.aldec.com/en/support/resources/multimedia/webinars/2187
  - OSVVM's Test Reports and Simulator Independent Scripting
    - https://www.aldec.com/en/support/resources/multimedia/webinars/2188
  - Advances in OSVVM's Verification Data Structures
    - https://www.aldec.com/en/support/resources/multimedia/webinars/2190
- Jump start your VHDL verification effort with training
  - Advanced VHDL Testbenches and Verification – OSVVM Boot Camp
  - https://synthworks.com/vhdl_testbench_verification.htm

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