

# Advanced VHDL for Synthesis and Verification

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**3-5 Days: 50% lecture, 50 % Lab**

**Advanced Level**

## **Overview**

Course materials come from the following core courses:

- Advanced VHDL Coding Styles for Synthesis (2 days)
- VHDL Testbenches and Verification (3 days)

## **Full 5-Day Course Outline**

### **Day 1, Synthesis Module AdvSyn1**

Subprograms for Synthesis  
Advanced Combinational Logic  
Advanced Sequential Logic  
Parameterizing Designs

### **Day 2, Synthesis Module AdvSyn2**

Advanced Arithmetic  
Architecting Hardware  
TxPort Statemachine  
Fixed and Floating Point Types

### **Day 3, Testbench Module TB1**

Testbench Overview  
Basic Testbenches  
Transactions and Subprograms  
Modeling for Verification  
VHDL IO

### **Day 4, Testbench Module TB2**

Lab Review: Testing w/ subprograms  
Transaction-Based BFM  
Execution and Timing  
Elements of a Transaction-Based BFM

### **Day 5, Testbench Module TB3**

Configurations and Simulation  
Management  
From Subblock to System Tests  
Creating Tests  
Modeling RAM

## **Customization Possibilities**

- 4 Day Class: AdvSyn1, AdvSyn2, Tb2, Tb3
- 4 Day Class: AdvSyn1, AdvSyn2, Tb1, Tb2
- 3 Day Class: AdvSyn1, AdvSyn2, Tb1
- 3 Day Class: AdvSyn1, AdvSyn2, Tb3 – only if previously took Tb2

Note it is also possible to include materials from the Intermediate VHDL Coding for Synthesis class.

# Advanced VHDL for Synthesis and Verification

## **Prerequisites**

Students taking this course should have significant experience designing and testing digital logic with VHDL or have taken the course:

**Intermediate VHDL for Synthesis and Verification – 3-5 days**

## **Intended Audience**

**Advanced VHDL for Synthesis and Verification** is recommended for experienced VHDL designers who need in-depth knowledge on synthesis and verification coding techniques.

## **Training Approach**

This hands-on, how-to course is taught by experienced hardware designers using a computer driven projector. We prefer and encourage student and instructor interaction. Questions are welcome. Bring problematic code.

## **Contact**

To schedule a class or for more information, contact:

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