Advanced VHDL
Coding Styles for Synthesis

2 Days: 50% lecture, 50 % Lab **Advanced Level**

Overview

An in-depth study of advanced VHDL RTL coding techniques for FPGA and ASIC design engineers.

Class topics focus on coding techniques, advanced language features (subprograms, generics, generate, packages), issue identification and problem solving. Lecture sections contain short exercises for immediate learning feedback. Labs, which account for approximately 50% of class time, give students the opportunity to experiment with different coding styles and problem solving techniques using the synthesis tool.

This class is the second half of VHDL Coding for Synthesis.

Intended Audience

Recommended for experienced VHDL designers who need in-depth knowledge on synthesis coding techniques.

Course Objective

Upon completion of this course, students will be able to:

- Use advanced VHDL constructs to simplify the coding process
- Understand and avoid problematic coding styles
- Identify and solve synthesis issues using VHDL coding techniques
- Force a synthesis tool to create the desired logic structure

Course Outline

Day 1, Module AdvSyn1

Subprograms for Synthesis
Advanced Combinational Logic
Advanced Sequential Logic
Parameterizing Designs

Day 2, Module AdvSyn2

Advanced Arithmetic
Architecting Hardware
TxPort Statemachine
Fixed and Floating Point Types

Advanced VHDL Coding Styles for Synthesis

Prerequisites

Students taking this course should have significant experience designing digital logic with VHDL or have taken the course:

Intermediate VHDL Coding Styles for Synthesis - 2 days

Other Recommended Courses

Students may also be interested in the following companion course:

VHDL Testbenches and Verification – 4 days

Customization

All of our courses can be customized to meet your specific needs. Either see our website or contact us for details.

Training Approach

This hands-on, how-to course is taught by experienced hardware designers using a computer driven projector. We prefer and encourage student and instructor interaction. Questions are welcome. Bring problematic code.

Contact

To schedule a class or for more information, contact:

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Learn VHDL from a designer's perspective with SynthWorks.