VHDL Introduction for Verilog Designers

1-4 Days: 50% Lecture, 50% Lab **Basic Level**

Overview

If you already have significant Verilog experience and need to learn VHDL, you may wish to take either a customized version of Comprehensive VHDL Introduction (3-4 days) or a customized version of a Quick VHDL Introduction (1-2 days). These are described in the two options that follow.

Option 1: Customize Comprehensive VHDL Introduction (3-4 days)

The underlying language concepts for VHDL execution, signal assignment, signal drivers/resolution, expression types and sizes are much different from the corresponding Verilog language concepts. To be successful with VHDL, you need to learn these concepts. Either a customized 3-day version or a full 4-day version of Comprehensive VHDL Introduction will help you achieve this goal. The class is fast paced and comes with an FPGA development board. One potential outline for the 3-day class is as follows:

Day 1

- A Quick Introduction
- Lab 1: Simple RTL and Testbench
- Data Types
- Operators
- Concurrent Statements
- Sequential Statements
- Lab 2: Clock and Reset
- Lab 3: RTL and Testbench

Day 2

- RTL Essentials
- Statemachine Coding Techniques
- Lab 4: RTL Code
- Data Objects
- Designing with VHDL
- Lab 5: Coding an FSM
- Lab 6: Creating Hierarchy

Day 3

- Testbench Essentials
- Subprograms
- Lab 7: Brute Force Testbenches
- Advanced Types
- VHDL IO (TextIO)
- Lab 8: Transaction-based Testbench
- Lab 9: Creating an FPGA (Synthesis and device programming).

Appendix to Course Materials

- RTL Code
- Lab Review
- Advanced VHDL Constructs
- Lab 10: UART Transmit Data Path
- Lab 11: UART Transmit Statemachine
- Lab 12: Multiplier Accumulator

Take Home Labs

- Digital Clock

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Option 2: Customize Quick VHDL Introduction (1-2 days)

Another option is to take either a customized 1-day version or the full 2-day version of Quick VHDL Introduction and follow it with an intermediate level training class, such as Intermediate VHDL Coding for Synthesis and VHDL Testbenches and Verification. We only recommended this for students with significant Verilog experience. The outline for the 1 day version could be as follows (note that this results in a long lecture day and little lab):

Day 1

A Quick Introduction
Data Types
Operators
Concurrent Statements
Sequential Statements
Data Objects
Designing with VHDL
Lab 3: RTL and Testbench

Prerequisites

None. Offered as a first course in VHDL. It is recommended that students are familiar with digital design.

Follow-On Courses

Students wishing to go beyond what they learned in this course should take either or both of the following courses:

VHDL Coding Styles for Synthesis - 4 days

VHDL Testbenches and Verification - 4 days

Training Approach

This hands-on, how-to course is taught by experienced hardware designers using a computer driven projector. We prefer and encourage student and instructor interaction. Questions are welcome. Bring problematic code.

Contact

To schedule a class or for more information, contact:

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Learn VHDL from a designer's perspective with SynthWorks.

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